CLAIMS

WHAT IS CLAIMED IS:

1. A method comprising the steps of:

defining a memory access quanta size by dividing a total memory bandwidth by a number of quanta, wherein the number of quanta is equal to an integer portion of one plus the total memory bandwidth divided by a quantity equal to the total memory bandwidth minus an amount of desired data needed plus one;

accessing the memory to retrieve an amount of retrieved data of the total memory bandwidth starting at a beginning of a quantum of the quanta in which a beginning of the desired data is located.

2. The method of claim 1 wherein the retrieved data is stored contiguously in a system memory space of the memory.

3. The method of claim 1 wherein the desired data is a contiguous block of data within a system memory space of the memory.

4. The method of claim 1 wherein the desired data is an asynchronous transfer mode (ATM) cell.

5. The method of claim 4 wherein the total memory bandwidth is 64 bytes.

6. A method comprising:

accessing within one memory access operation a plurality of storage devices such that a first portion of the plurality of storage devices is accessed at a first hardware memory address and a second portion of the plurality of storage devices is accessed at a second hardware memory address adjacent to the first hardware memory address.

7. The method of claim 6 wherein the plurality of storage devices are separate storage devices provided with respectively separate address buses.

8. The method of claim 6 wherein the plurality of storage devices are implemented within a larger storage device, the larger storage device comprising an input to select an addressing mode.

9. The method of claim 8 wherein the addressing mode allows selection of different hardware memory addresses among the plurality of storage devices for a same memory access operation.

10. A system comprising:

a first storage device;

a second storage device; and

a processor coupled to the first storage device and to the second storage device, the processor configured to access within one memory access operation, a first hardware memory address of the first storage device and a second hardware memory address of the second storage device, the second hardware memory address being adjacent to the first hardware memory address.

11. The system of claim 10 wherein the first storage device and the second storage device are separate storage devices provided with respectively separate address buses.

12. The system of claim 10 wherein the first storage device and the second storage device are implemented within a larger storage device, the larger storage device comprising an input to select an addressing mode.

13. The system of claim 12 wherein the addressing mode allows selection of different hardware memory addresses among the first storage device and the second storage device for a same memory access operation.

14. A memory system comprising:

a plurality of memory banks accessible via a plurality of modes of access to allow selection among a plurality of predefined memory access starting points, wherein the predefined memory access starting points occur at intervals of less than a total memory bandwidth.

15. The memory system of claim 14 wherein the plurality of memory banks are accessible via burst access.

16. The memory system of claim 15 wherein the total memory bandwidth is equal to the burst size.

17. The memory system of claim 14 wherein the predefined memory access starting points occur in the memory banks as a function of a size of a desired data block to be accessed.

18. The memory system of claim 14 wherein the amount of desired data is stored contiguously within a system memory address space of the memory system.

19. The memory system of claim 17 wherein the amount of desired data is an asynchronous transfer mode (ATM) cell.

20. The memory system of claim 14 wherein the predefined memory access starting points occur in the memory banks at intervals of the total memory bandwidth divided by a number of the intervals containing an amount of desired data, wherein the number of the intervals is equal to an integer portion of one plus the total memory bandwidth divided by a quantity equal to the total memory bandwidth minus the amount of desired data needed plus one.